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NANOSECOND PULSE LOW-POWER AMPLITUDE-TO-TIME CONVERTER AND ASSOCIATED LINEAR GATE CIRCUITS

BY

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GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

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INTRODUCTION

During the development of a pulse height analyzer for nanosecond pulses produced by satellite and balloon-borne cosmic ray detectors, a need arose for both a low-power pulse-gating circuit and an amplitude-to-time converter. It was required that each device respond to pulses as short as 200 nanoseconds. In addition, linear operating characteristics were needed over a range of input pulse amplitudes from 10 millivolts to 5.12 volts.

Subsequent effort produced a circuit that met these requirements, and it is believed that the achievement represents a sufficient advance over existing state of the art to warrant a brief report on its configuration and operation.

PULSE HEIGHT ANALYZER

The general form of a pulse height analyzer for one linear parameter is shown in Figure 1. The circuits are designed to provide a clock-pulse-train output in which the number of pulses is proportional to the input-pulse amplitude.

A trigger pulse from the logic circuitry (not shown) turns on the linear gate driver which "unblocks" the linear gate to accept the desired logic-selected pulse input. In the absence of a logic trigger pulse the linear gate remains in the "blocked" condition.

The linear operating range of the system is from 10 millivolts which delivers an output pulse count of "1", to 5.12 volts for an output pulse count of 512.

The circuitry within the dashed line of Figure 1 is the subject of this report.

Linear Gate

As shown in Figure 1, input pulses from the cosmic ray detector pass through shaping circuits. These circuits delay the pulse long enough to allow time for the linear gate to be placed in the "unblocked" condition. Figure 2 shows the timing relationship between the input pulse from the cosmic ray detector and the linear gate turn-on pulse from the linear gate driver.

The linear gate must meet two requirements in addition to providing a linear in-out relationship: (1) The attenuation of the input pulse from the cosmic ray detector must be negligible when "unblocked." (2) When "blocked," the attenuated output must be less than 5 millivolts for all pulses appearing across the gate input.

The design of this linear gate (Figure 3) is based on the "Bright" circuit, used extensively in low-frequency chopper and commutator applications, wherein the unblocking drive pulse is applied in the "inverted beta" mode to minimize transistor emitter-to-collector offset voltage. In this mode the driving currents I_d from T1 are sent through the base-collector junctions rather than the base-emitter junctions, and the normally high forward beta then becomes a high inverse beta. Under these conditions the transistor emitter-to-collector offset voltage is reduced from 10 millivolts to about 1 or 2 millivolts, and if the transistors are connected back-to-back the offsets are of opposite polarity and cancel out. The total in-line offset can be made negligible for all input pulses over 10 millivolts by transistor selection and matching inverted offsets.

For the "blocked" requirement, Q1 in the linear gate is cut off; unwanted input pulses then drive it further into the back-bias region and therefore do not pass through. Any unwanted capacitance coupling between input and output is minimized by careful circuit layout and by selecting transistors with small emitter-collector capacitance. The small portion of the unwanted input pulse that may leak through is effectively shunted to ground by the output capacitor. This capacitor may be considered as an impedance divider in series with the two small transistor junction capacitances; hence it need not be large for effective shunting of the leak-through.

By limitation of the linear gate "unblocked" time to about 3 times the input pulse width, most of the noise originating ahead of the gate is kept out of the amplitude-to-time (A-T) converter.

Another source of noise is the turn-on and turn-off spikes which may be coupled into the output pulse line from the driving current I_d. Small positive-going spikes will not be seen by the A-T converter, but large positive spikes will cause gross distortion of the input pulse and therefore must be reduced. Negative going spikes must be kept considerably below the "count of 1" level of 10 millivolts. This spike reduction is effected primarily by keeping the primary and secondary windings of the linear gate transformer T1 on opposite sides of the core, thus reducing the interwinding capacitance.

When selecting transistors for use in the linear gate, the available turn-on drive from the driving source must be considered in relation to the facing betas — in this case an inverse beta because the drive is applied between base and collector. Where minimal turn-on drive is present, transistors with a minimum

inverse beta of 5 should be selected to ensure passage of the signal pulse through the gate without attenuation. The drive current will also generate voltage offsets across the base-collector junction but these are of opposite polarity and will cancel out.

Linear Gate Driver

The design of the driving "turn-on" source for the linear gate transformer T1 is quite important if spiking is to be kept at a minimum. Figure 4 shows the linear gate driver, which is a common-emitter blocking oscillator operating in the transformer-controlled mode. The linear gate is fed from balanced windings (which reduces spiking) on the driver transformer with 100 ohm series resistors to prevent overdrive and resultant ringing. To limit the blocking oscillator (B.O.) feedback and keep ringing low, the value of R3 should be as high as is practical.

It will be noted that power is consumed only when the blocking oscillator is triggered. As a result of this, power drain is negligible in systems where the linear gate is only required to be unblocked for a small fraction of the total time.

Pulse Amplitude-to-Time Converter

Operation—After a pulse is accepted by the linear gate it enters the amplitude-to-time converter which converts the pulse amplitude variations to time-width variations. This converter circuit, shown in abbreviated form in Figure 5, is a form of pulse stretcher wherein a temperature-stable silver-mica capacitor C_t is charged to the peak pulse amplitude through a series transistor and diode, and then is permitted to discharge at a controlled rate through a constant current source.

The input pulse to be measured appears on one side of the comparator—an emitter-coupled pair consisting of Q1 and Q2—that supplies drive to Q5 and charges the capacitor through diode CR9. The loop returns this capacitor voltage to the opposite side of the comparator in a common-mode nulling arrangement. With zero charge on the capacitor a large error voltage is developed at the collector of Q1 and the capacitor charges rapidly to the peak amplitude of the pulse, bringing the error voltage to zero. Transistor Q5 ceases conducting and CR9 becomes reverse-biased as the collector of Q5 rises to +6 volts.

The capacitor retains this amplitude-proportional charge until a predetermined time when a turn-on pulse fed into the discharge switch initiates the linear ramp discharge. At the end of the ramp rundown, Q5 and CR9 recover rapidly from cut-off and the collector of Q5 reverts to a negative voltage. Thus, two well defined time-domain points are available for generating a square wave, the width of the generated pulse being pulse-amplitude dependent and suitable for gating a

succeeding oscillator circuit. The gated pulse train from the oscillator represents the digital conversion of the analog information contained in the input pulse.

Circuit Description—Because Q1 has to respond to pulse levels down to 10 millivolts, it operates "wide open" with its base clamped to ground by dc restorer CR1-CR2 and its forward bias is set by the +12 volts on R6. The potential on the base of Q2 will follow that on the base of Q1. Transistor Q5 is held quiescently "ON" by the collector current of Q1 but its collector voltage is prevented from bottoming by diode clamp CR9. Hence in the absence of an input pulse, the collector of Q5 can never go more negative than two diode voltage drops below ground, and idles at about -1.2 volts. Thus the collector of Q5 is constrained not to exceed the negative pulse excursion appearing on the base of Q1.

The wide-open quiescent condition of the converter partially sets the input pulse requirements. First, ingress must be blocked at all times except when the coincident pulse is present; otherwise noise and non-coincident pulses might override the measured pulse on C_t and inject an error voltage. Second, the measured pulse must have a reasonably fast tail-off to hasten the cut-off of Q1. This last requirement is necessary because Q1 is only completely cut off when Q2 can dominate the emitter current through R6: even under comparator null balance, Q1 continues to dribble current into the charge capacitor until the tail on the base of Q1 drops below the ramp level on the base of Q2. Transistor Q1 is then cut off and remains insensitive to any input pulses below the ramp level of the charged capacitor voltage on the base of Q2.

The linear gate effectively blocks any overriding noise and pulses. The effect of an extended input pulse tail-off is a slow turn-off of Q5 with resultant slow collector rise to +6 volts as shown in Figures 6a and 6b. This may mask low-level pulse measurements if the turn-on ramp-rundown pulse is early, since a portion of the ramp discharge may be lost before the collector voltage at Q5 can rise high enough to form a shaped pulse in the shaper module. Under certain conditions, such as low-level input pulses having extended tail-off, Q5 may not build up any charge on C_t at all. However, shaping of the pulse tail-off is easily achieved.

When the amplitude of very short fast pulses is to be measured, the problem becomes one of charging the timing capacitor to the input pulse peak amplitude and bringing the difference amplifier to null within the pulse-peak-duration period. If the timing capacitor is too large or the loop response time too long, the input pulse peak will have passed before amplitude comparison can be made; and the capacitor charge will then also depend on pulse width instead of solely on pulse amplitude—an undesirable condition. This is indicated in Figure 7a where a too large RC product is used for a given minimum width of a pulse whose amplitude

is to be measured. Here the voltage E_n appearing on the base of Q3 is used to null against the input pulse E_{in}, but the capacitor voltage has not reached this value and the capacitor still charges for the duration of the input tail-off, finally reaching a value E_{ct}. The E_n voltage, after a small overshoot, comes to rest at a new value E_r equal to E_{ct}. This value E_{ct} is not a true measure of the input amplitude because a second pulse of equal amplitude but longer duration (Figure 7b) would permit C_t to charge to the peak level, thus producing a greater output count.

The purpose of the small resistor (Figure 8) in series with charge capacitor C_t is to retard the phase of the feedback voltage from the 90° lead it receives across the capacitor. Without this series resistor, severe ringing occurs; with too large a resistor, the capacitor will not charge to the peak level of the pulse.

There is also a limit on the minimum value of the charge capacitor that may be used; this is set by the discharge circuit shown in Figure 8. Transistor Q4 is a grounded base switch which is controlled by the turn-on pulse emanating from the logic circuitry. A level of -3 volts at CR5 will hold Q4 open. A +6 volt level will open CR5 and permit the charge on C_t to run down through Q4 and R11. The bottom of R11 is set to a constant voltage of about +7 volts by reference diode CR3 (returned to ground through offset-temperature diode CR4 which compensates against the base-emitter offset of Q4). A linear ramp rundown is achieved because the collector current of Q4 is independent of the voltage across C_t. The ramp rundown is set by R11 (for a given E ref) and is determined by the frequency of the oscillator to be gated and the converter input sensitivity. In this case the sensitivity is 10 millivolts/count and the oscillator frequency is 500 kHz. The ramp rundown is then 10 millivolts/2 microseconds. For a maximum input of 5.12 volts the ramp time is 5.12/0.01 x 2 = 1.024 milliseconds, and the discharge current through the transistor for this length of time for a 2000 pf capacitor is 10 microamperes. This charge on C_t must also hold Q3 in conduction while Q4 is waiting for the ramp turn-on pulse and this imposes another drain on the charge on C_t. Hence, for a 10 microampere ramp discharge current all other drains on the charge bus must be kept much smaller than this to maintain acceptable linearity and temperature stability. A C_t of 2000 pf appears to be the minimum usable value for the present circuitry.

The actual circuitry of the linear gate, linear gate driver, and amplitude-to-time converter used in the satellite is shown in Figures 9, 10, and 11. Each schematic represents an individual module with components arranged in "cordwood" fashion and welded to a matrix. External leads permit welding to a mother matrix for final assembly of the module interconnections.

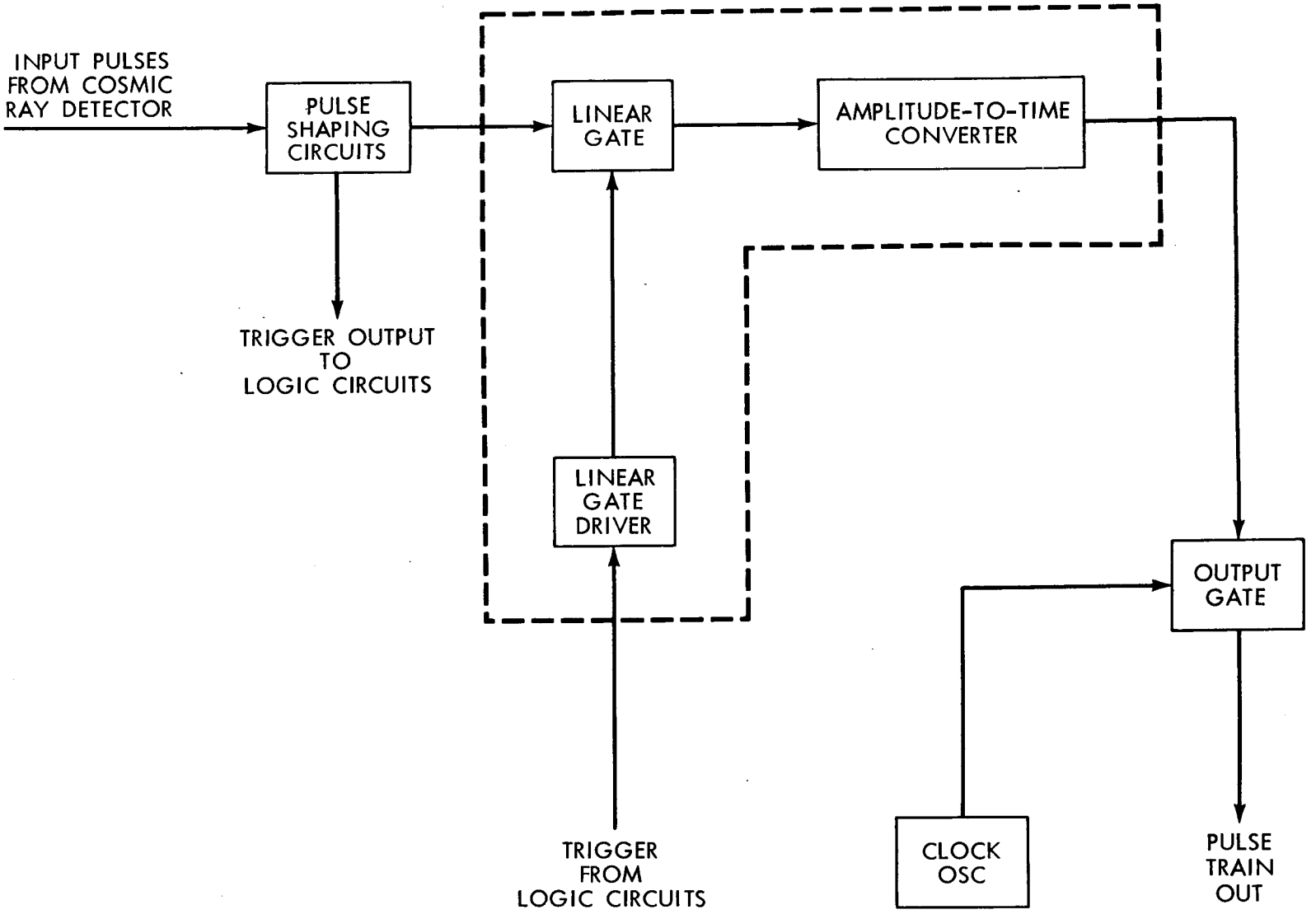


Figure 1. Pulse Height Analyzer (Typical linear measurement channel)

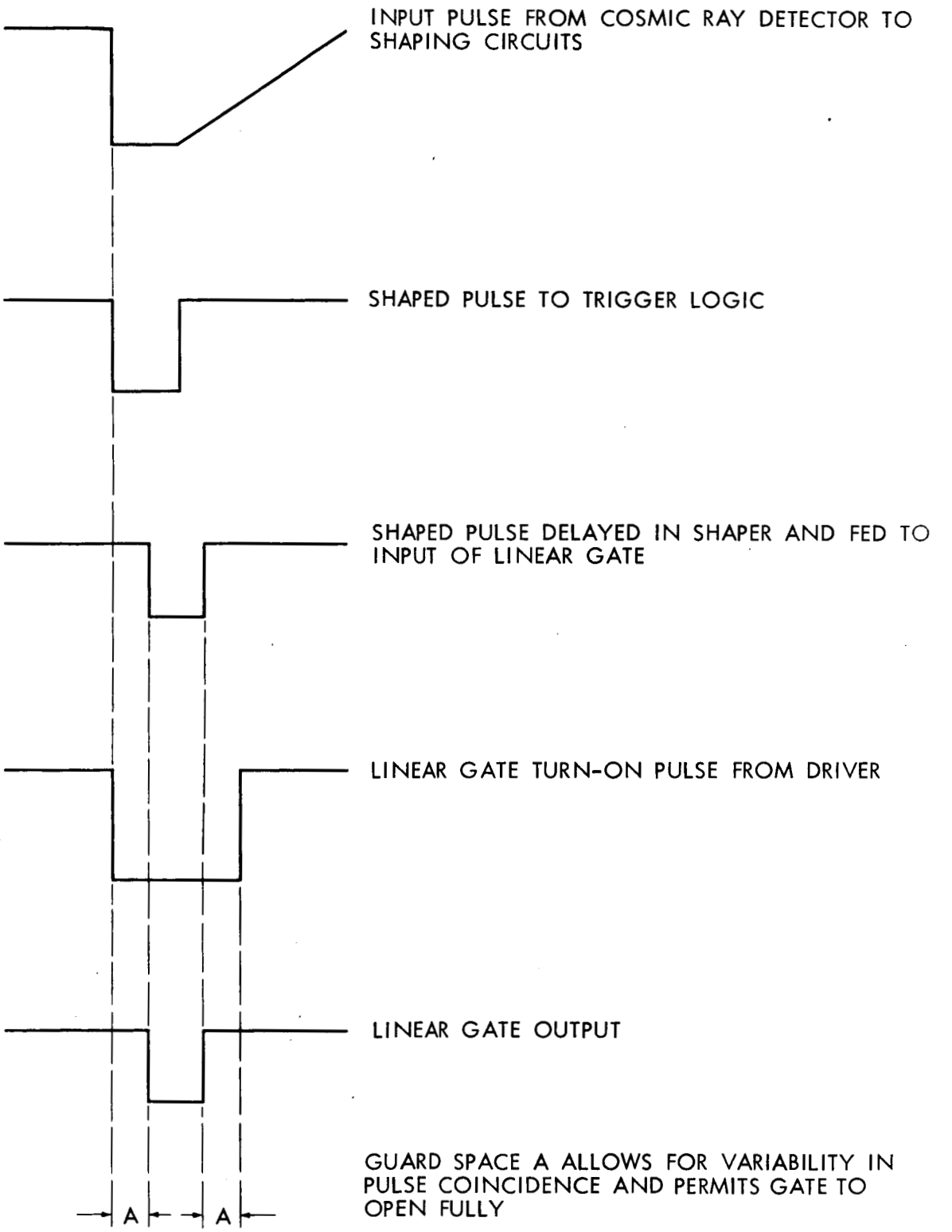


Figure 2. Pulse Timing Diagram Showing Relationship Between Input Pulse and Linear Gate Turn-On Pulse

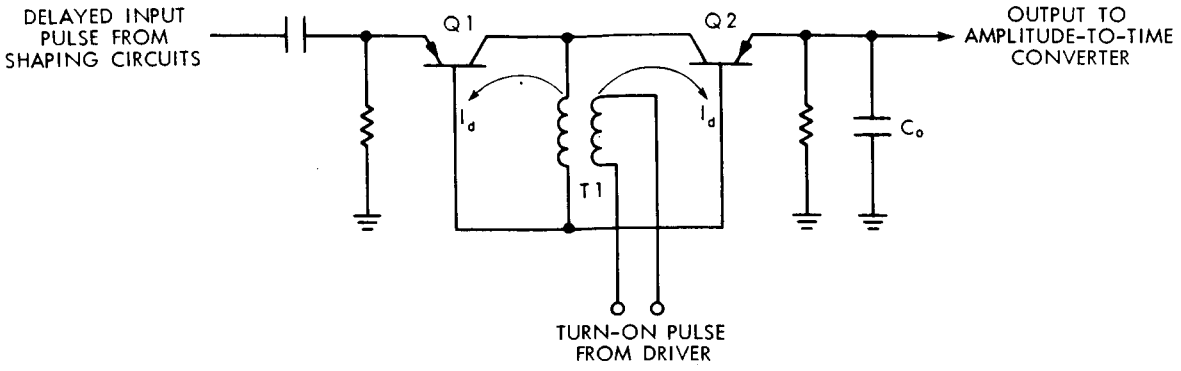


Figure 3. Linear Gate Schematic Diagram

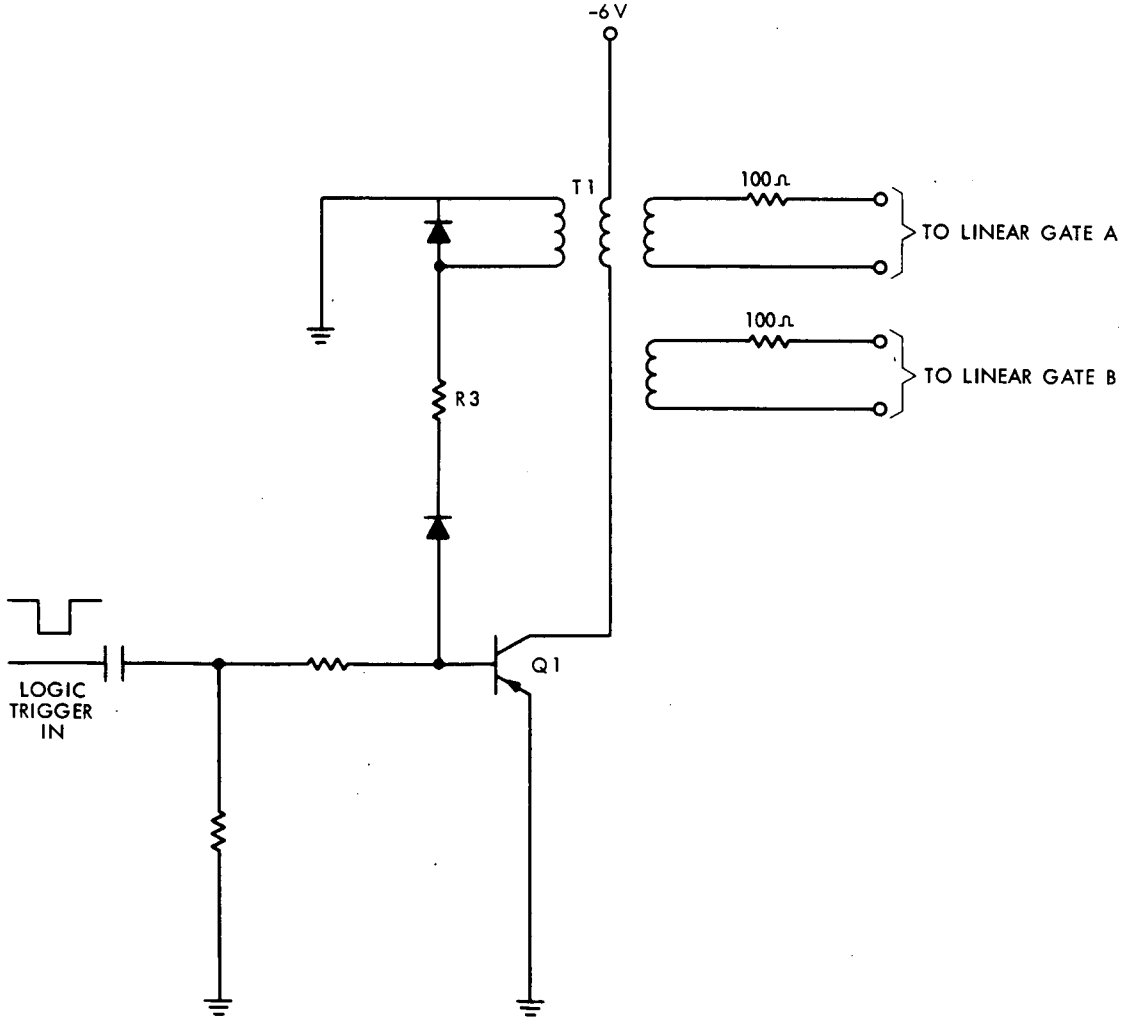


Figure 4. Linear Gate Driver

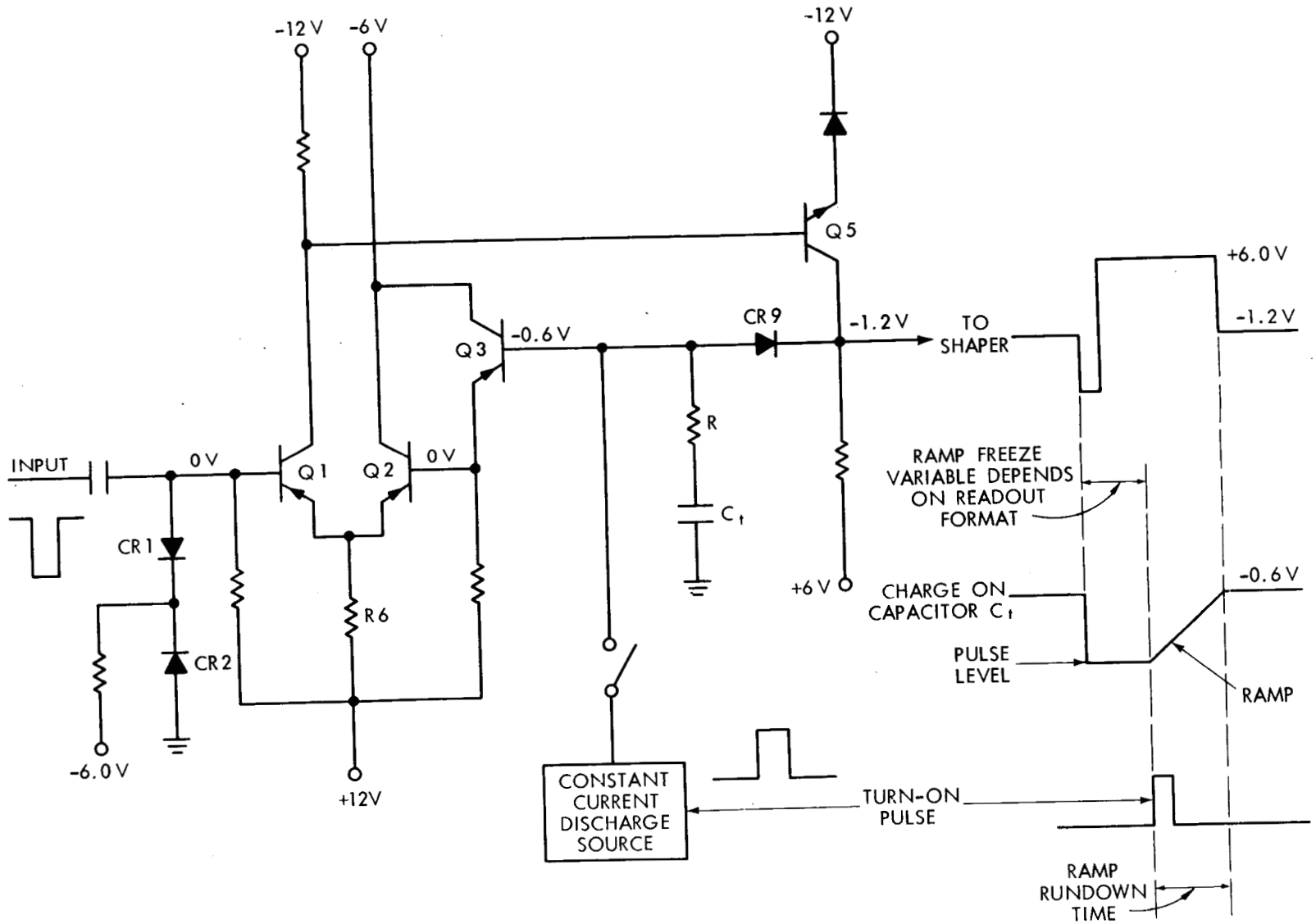


Figure 5. Converter Circuit Showing Input Pulse Amplitude Conversion to Capacitor Ramp Run-Down Time

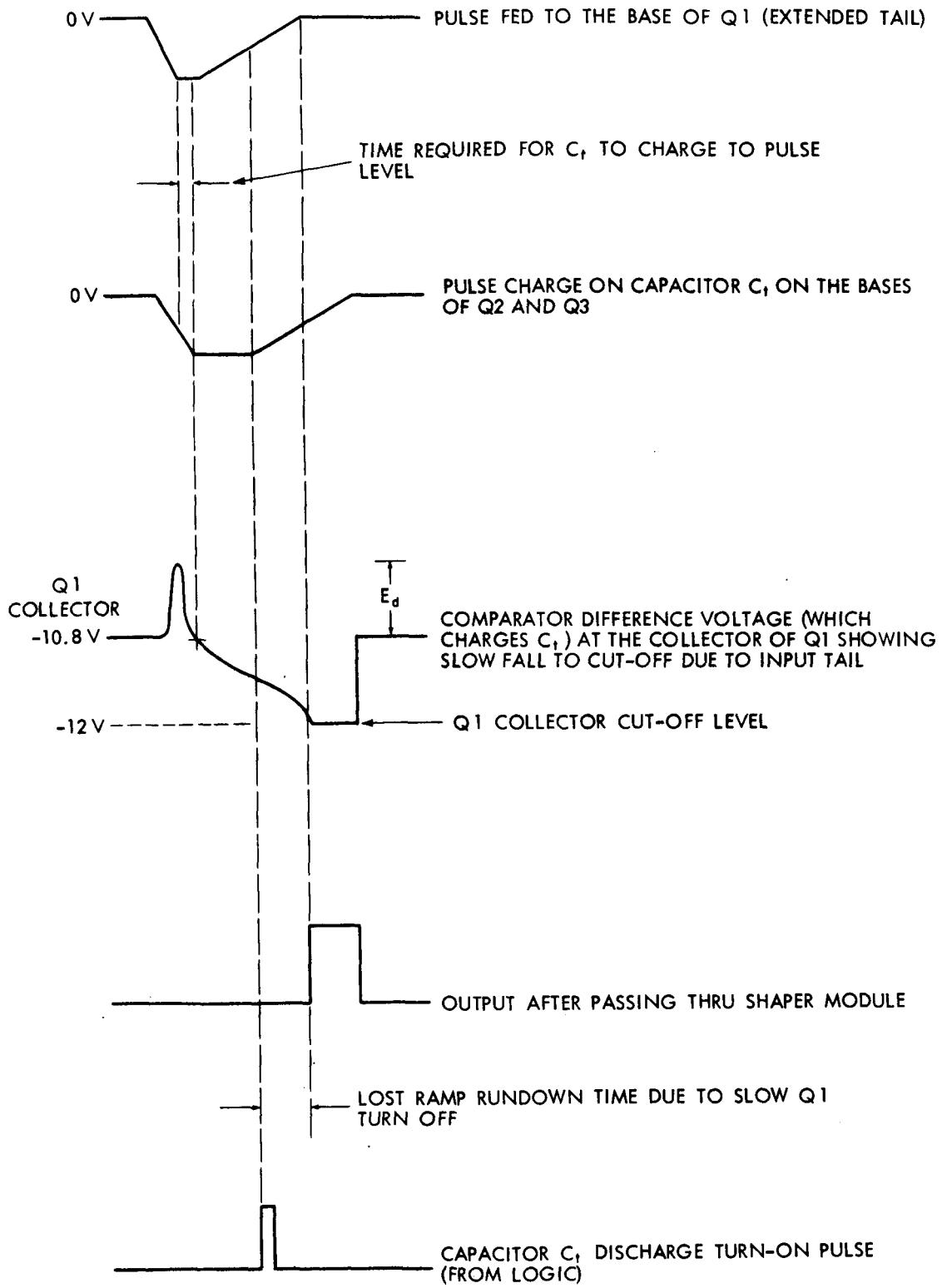


Figure 6a. Effect of Long Tail-Off of Input Pulse (Loss of low counts)

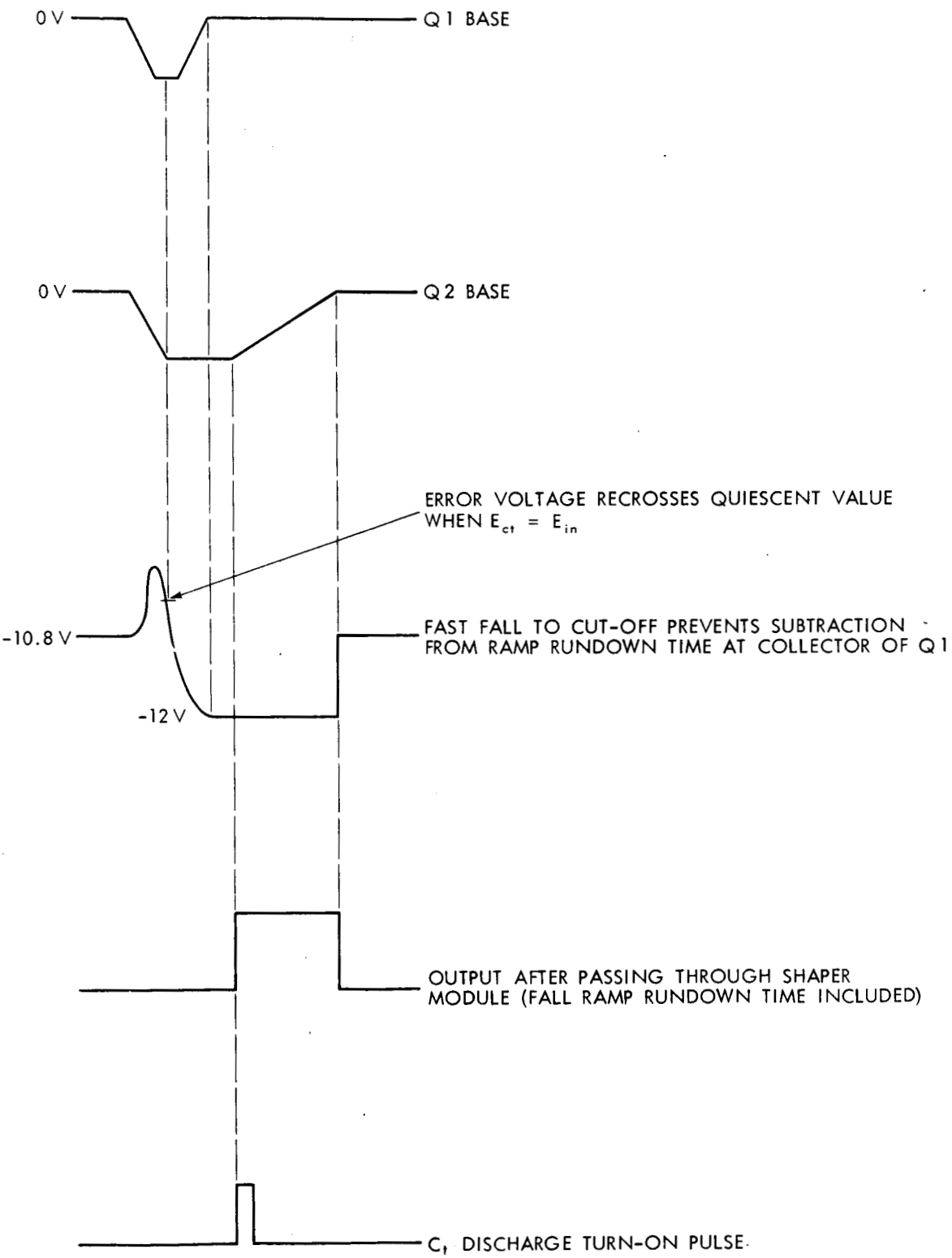


Figure 6b. Fast Input Tail-Off Necessary to Obtain True Conversion

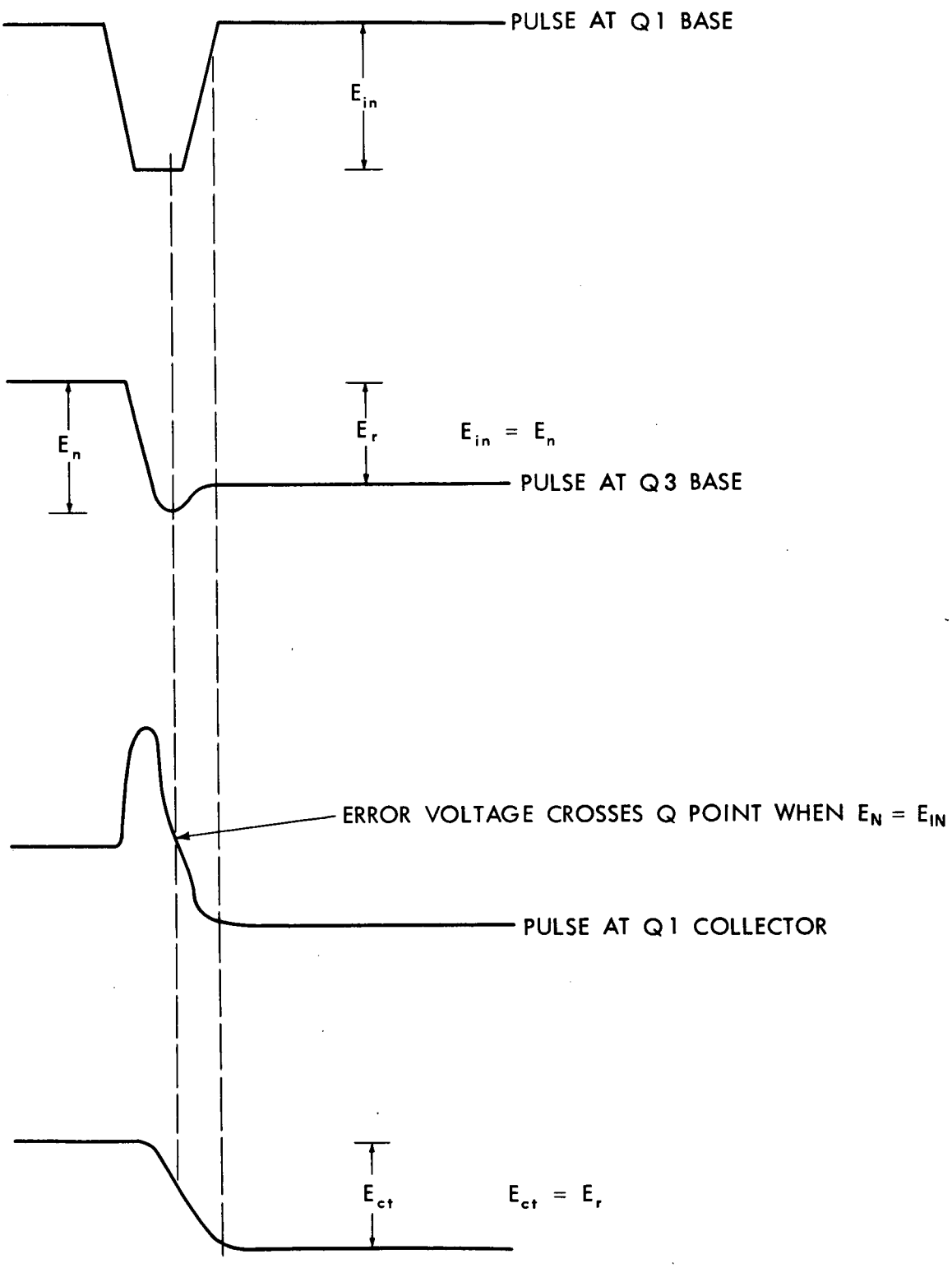


Figure 7a. Pulse Charge on C_t versus Input Pulse when RC is Too Large

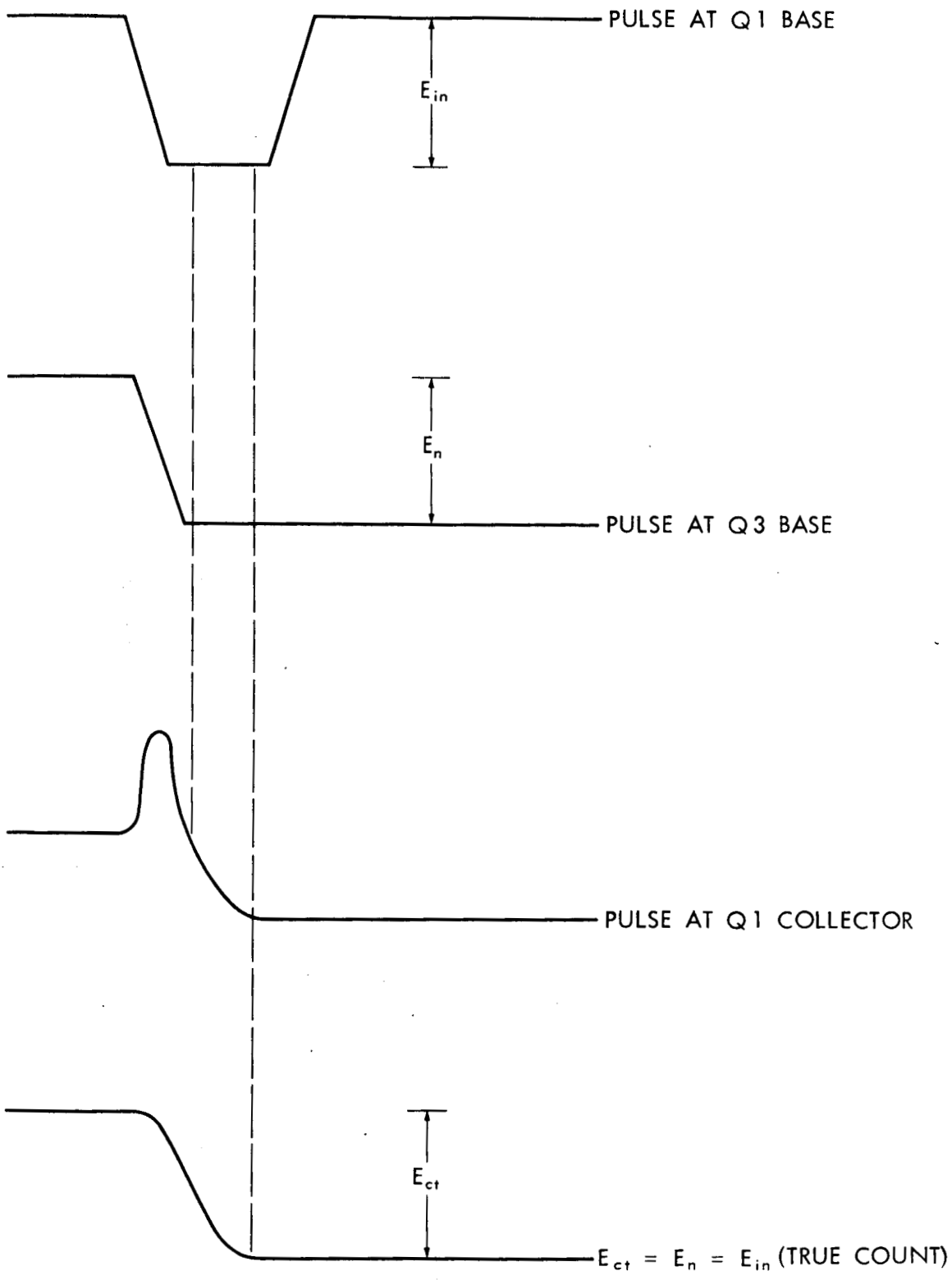


Figure 7b. Input Pulse Duration must be Longer than RC Time for a True Count

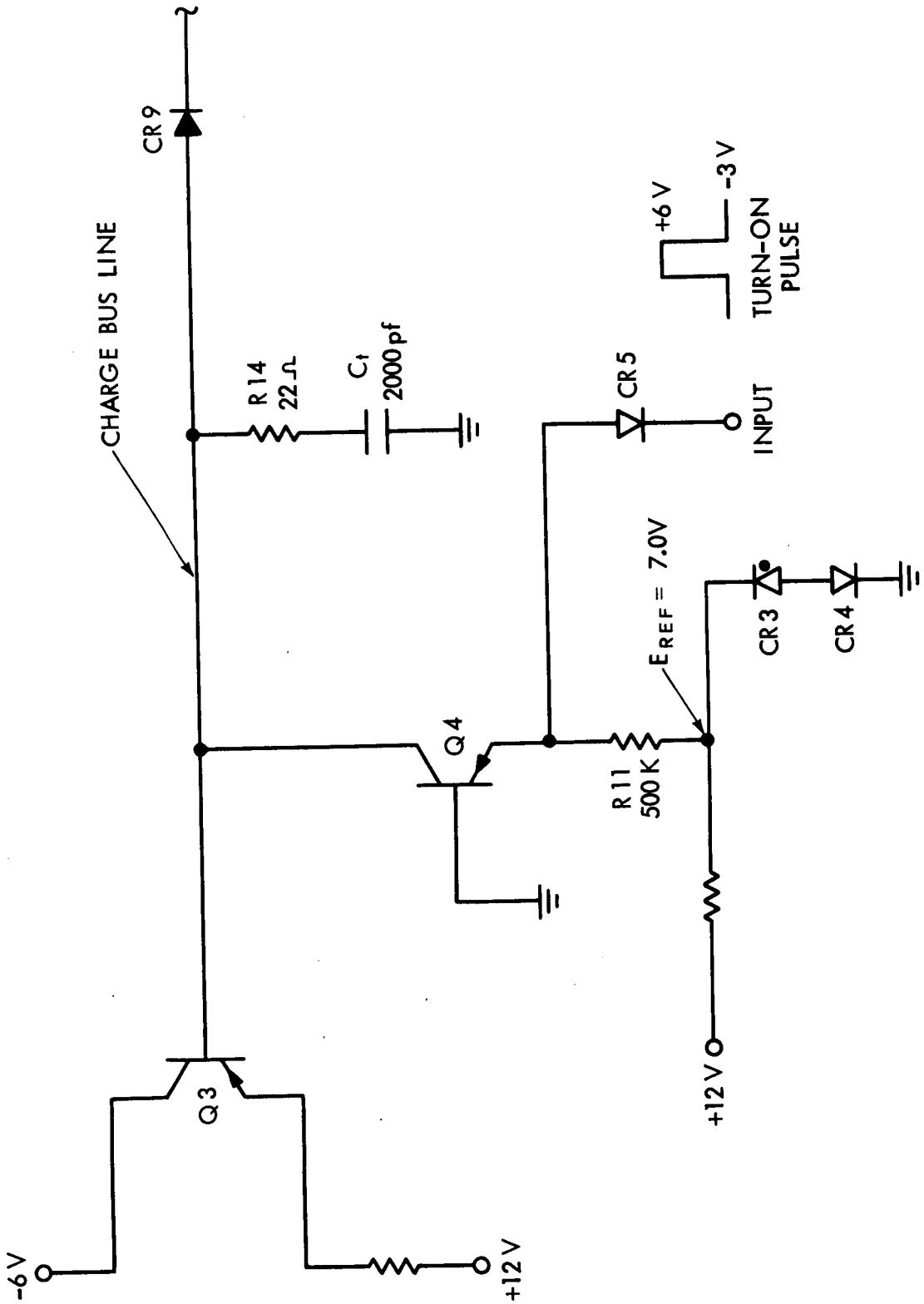
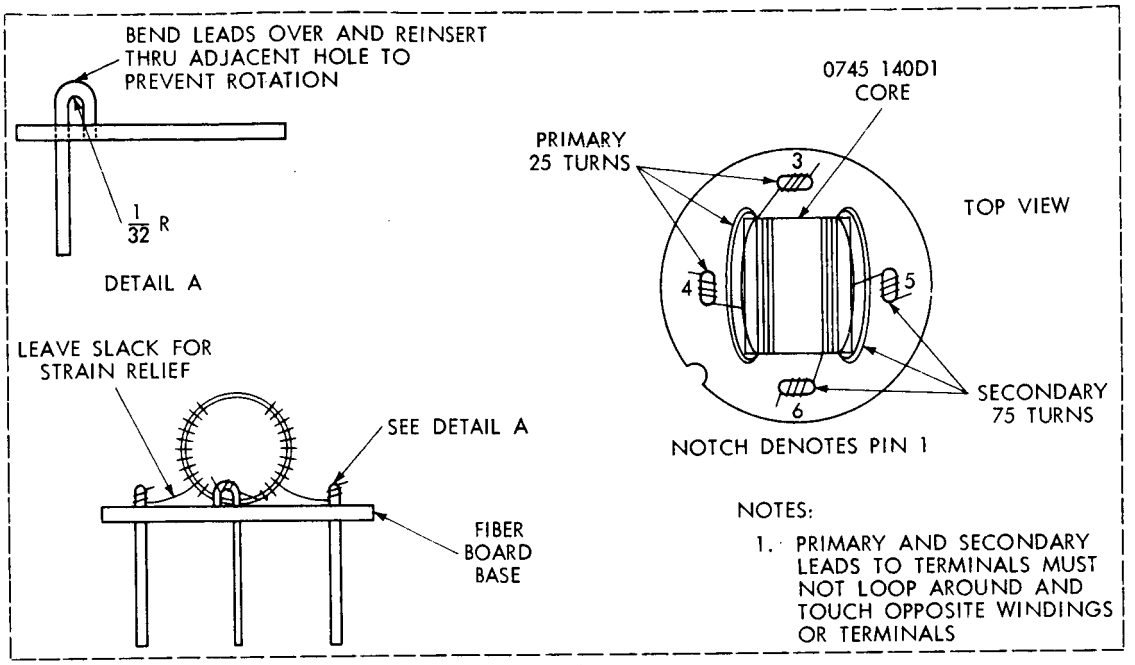


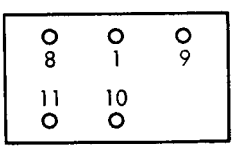
Figure 8. Constant-Current Discharge Source for Capacitor C_t



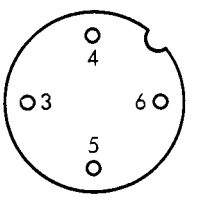
T1

PIN CODE

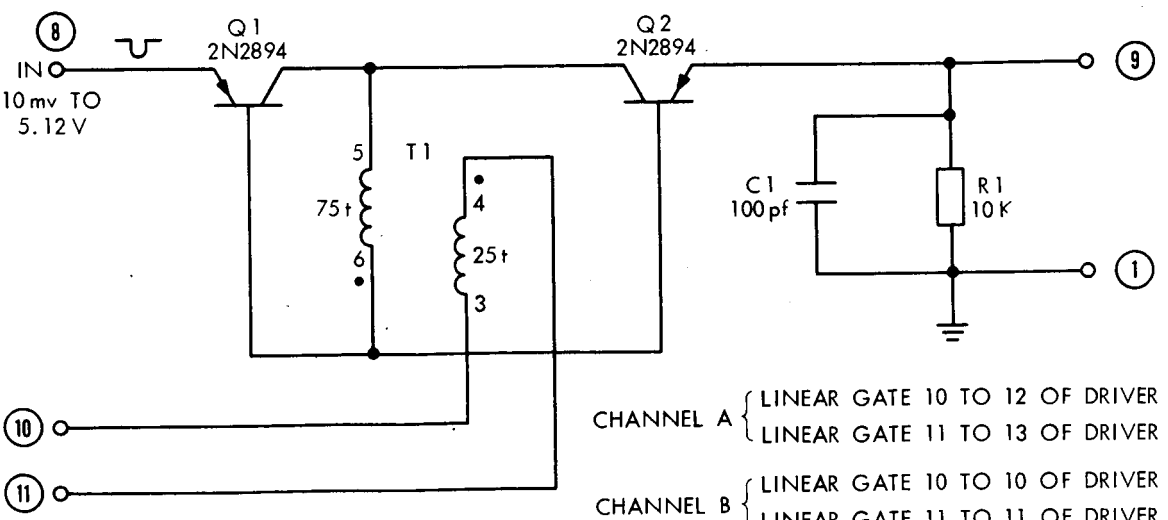
1. GRD
8. IN
9. OUT
10. TRANSFORMER INPUT
11. TRANSFORMER INPUT



PIN LAYOUT



T1



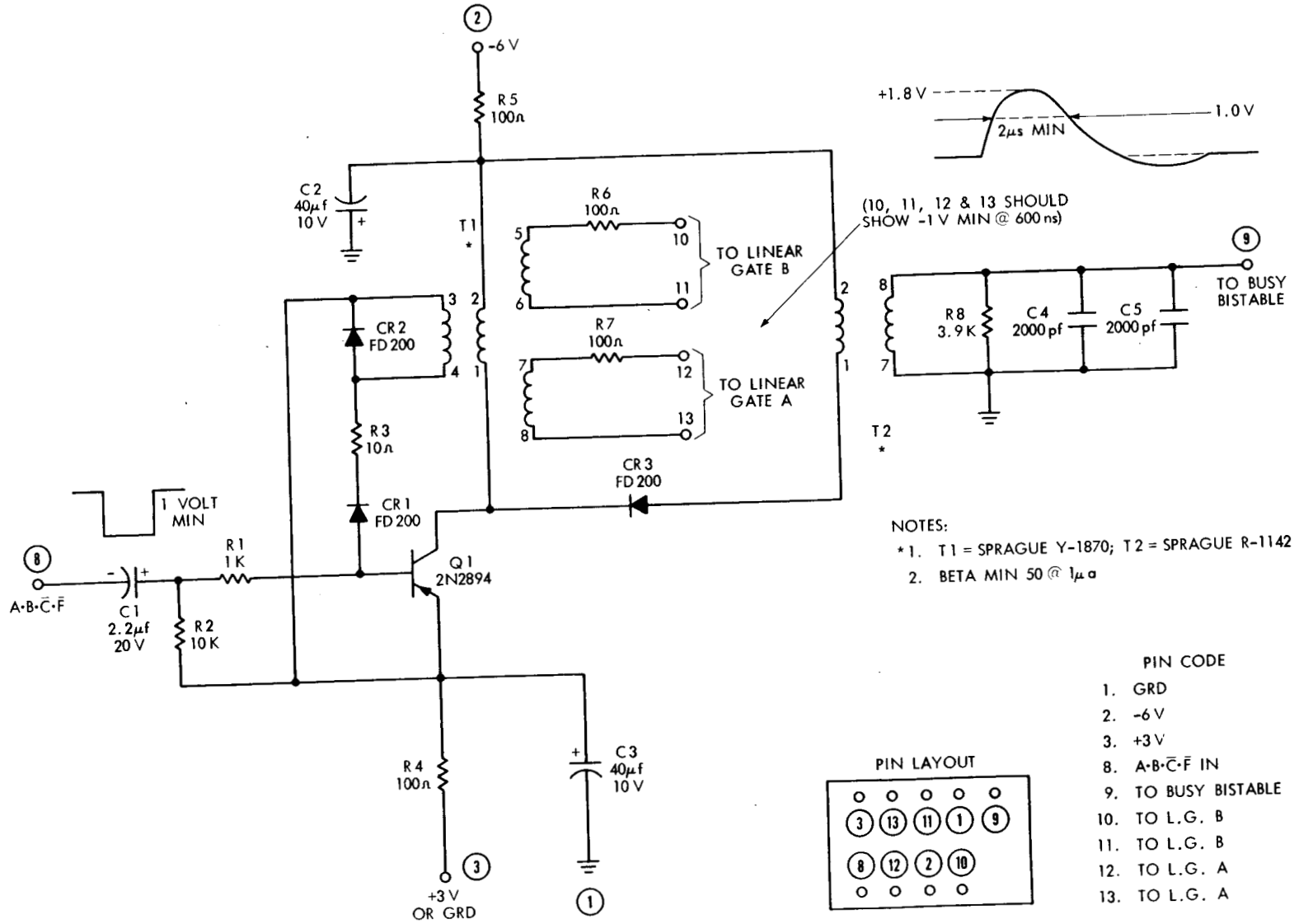
CHANNEL A { LINEAR GATE 10 TO 12 OF DRIVER
LINEAR GATE 11 TO 13 OF DRIVER

CHANNEL B { LINEAR GATE 10 TO 10 OF DRIVER
LINEAR GATE 11 TO 11 OF DRIVER

NOTES:

1. T1 = (REF DWG NO GB-IMP-1154-058) OR (R-1174 SPRAGUE)

Figure 9. Linear Gate Schematic Diagram



NOTES:

*1. T1 = SPRAGUE Y-1870; T2 = SPRAGUE R-1142

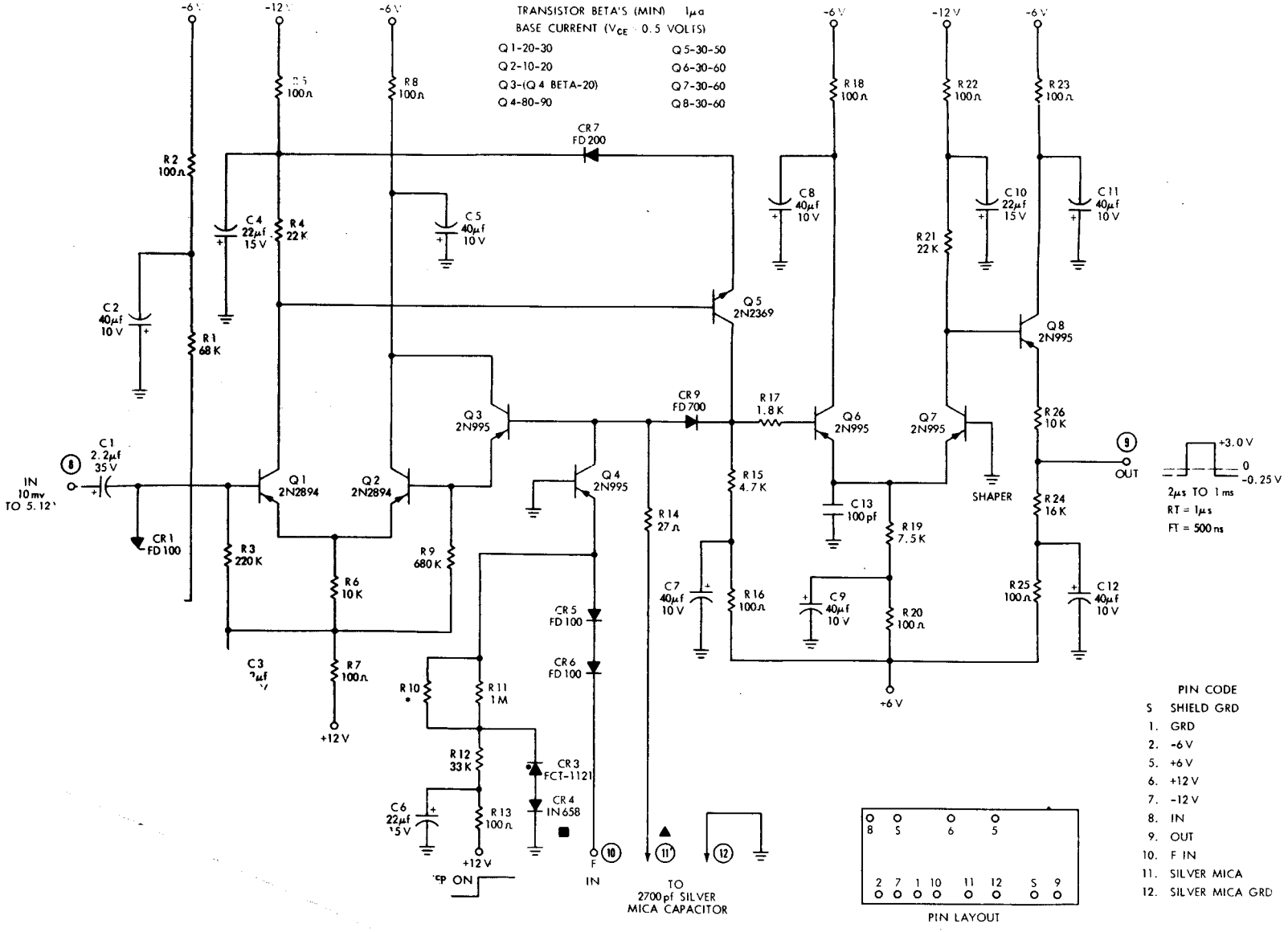
2. BETA MIN 50 @ 1μa

PIN LAYOUT

PIN CODE

1. GRD
2. -6 V
3. +3 V
8. A·B·C̄·F̄ IN
9. TO BUSY BISTABLE
10. TO L.G. B
11. TO L.G. B
12. TO L.G. A
13. TO L.G. A

Figure 10. Linear Gate Driver Schematic Diagram



'tude-to-Time Converter Schematic Diagram